Yixiao Du

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EDUCATION

08/2020 - present — **Cornell University** — Ithaca, NY
- School of Electrical and Computer Engineering
- MS/Ph.D. in Electrical and Computer Engineering

08/2019 - 08/2020 — **Cornell University** — Ithaca, NY
- School of Electrical and Computer Engineering
- M.Eng. in Electrical and Computer Engineering
- Overall GPA: 4.038/4.25
- Converted to MS/Ph.D. track in 08/2020

09/2015 - 06/2019 — **University of Electronics Science and Technology of China (UESTC)** — Chengdu, Sichuan, China
- School of Electronic Science and Engineering (National Exemplary School of Microelectronics)
- Bachelor of Engineering in Microelectronics Science and Engineering
- Overall GPA: 3.91/4.00

RESEARCH EXPERIENCE

06/2020 - present — **Computer Systems Lab, Cornell University** — Ithaca, NY
Graduate Research Assistant

Focusing on FPGA acceleration of sparse workloads using high-level synthesis. Interested in providing system-level solutions to sparse HPC applications.

- **HiSparse: High-performance sparse linear algebra on HBM-FPGAs**
  Explored approaches to perform sparse matrix-vector multiplication (SpMV) on Xilinx Alveo U280 FPGA. Paper [1] appeared in FPGA'22.
- **GraphLily: graph linear algebra overlay on FPGAs**
  Built a graph processing system using Xilinx Alveo U280 FPGA that exposes a GraphBLAS interface. Paper [2] appeared in ICCAD'21.

06/2018 – 06/2019 — **The Anti-irradiation Products Design Lab, UESTC** — Chengdu, Sichuan, China
Research Assistant

Assisted in design and testing of anti-irradiation VLSI standard cells. Responsible for the maintenance of lab-designed devices.

- **Anti-irradiation Device Modeling and Simulation**
  Modeled and simulated the behavior of devices using a silicon on insulator technology. The simulated results were used in the VLSI design of anti-irradiation logic gates.
- **Programmer for Anti-irradiation PROM Devices**
  Upgraded a pre-designed programmer to fit the newly designed PROM devices by modifying the MCU program and replacing parts on the PCB. Also in charge of the maintenance of the PROM programmer.

PUBLICATIONS

[1] **Y. Du**, Y. Hu, and Z. Zhang, High-Performance Sparse Linear Algebra on HBM-Equipped FPGAs Using HLS: A Case Study on SpMV, *International Symposium on Field-Programmable Gate Arrays (FPGA)*, Feb./Mar. 2022.

[2] Y. Hu, **Y. Du**, E. Ustun, and Z. Zhang, GraphLily: Accelerating Graph Linear Algebra on HBM-Equipped FPGAs, *International Conference on Computer Aided Design (ICCAD)*, Nov. 2021.

TEACHING EXPERIENCE

01/2022 – 05/2022	**ECE/ENGRD 2300: Digital Logic and Computer Organization, Cornell University** *Head Teaching Assistant* **Received the ECE Outstanding Ph.D. TA Award** - Design lab assignments and exam questions - Hold office hours and lab sessions - Lead tutorial sessions and exam review sessions	Ithaca, NY

SELECTED PROJECTS

10/2019 – 05/2020	**FPGA acceleration of CNN-based power estimation** *Cornell ECE M.Eng. Design Project* **Individual project** - Created a workflow which integrates an RTL hardware emulator, an HLS machine learning accelerator and C++ software - Built a converter to format a PyTorch model into Caffe, which the accelerator accepts	Ithaca, NY
11/2018 - 05/2019	**Design of speech recognition system based on FPGA** *Undergraduate Final Project (with thesis)* **Individual project** - Designed a voice filtering, sampling, and recording system - Extracted MFCC characteristics (based on FFT) and compare with pre-recorded voice syllables - Achieved an accuracy of 90% in simulation	Chengdu, Sichuan, China
10/2017 – 03/2018	**Feedback suppressor using FPGAs** *Project of the National Students' Platform for Innovation and Entrepreneurship Training Program* **Leader of the project team** - Designed a feedback suppressor for low-end audio devices, such as handheld speakers, to prevent howling (happens when the microphone is pointed to the speaker). - The core part of the suppressor was an FPGA-based digital attenuator that enabled automatic gain control for audio devices. - The project was rated as Excellent (top 10%) by the university.	Chengdu, Sichuan, China

ACTIVITIES

07/2016	**Simulated start-up running contest** *Member of the study tour organized by the university* - Attended lectures about running a start-up - The team won the 3rd place with the idea of Graphene Battery	Fremont, CA
09/2015 – 09/2017	**Design Center of the Student Union of UESTC** *Member (2015 – 2016), Associative Director (2016 - 2017)* - Designed posters, banners, and magazines for the Student Union - Organized the 6th and 7th campus-wide microfilm contest	Chengdu, Sichuan, China

SKILLS

- Designing complex hardware systems using high-level synthesis
- Digital Logic and Computer Architecture, rich experience on FPGAs
- Building and testing digital hardware systems using VHDL/Verilog
- Building software programs using C, C++, or Python
- Familiar with Linux command-line prompt
- Familiar with VLSI design tools
- Design tools: Adobe Photoshop, Illustrator